Fault Isolation for ICs and Microelectronics

Technology development, yield learning, and reliability engineering are critical to the microelectronics and now nanoelectronics business. All are highly dependent on fault isolation and failure analysis. With higher density packaging, transistor counts into the billions, scaling below 22 nanometers, and new materials however, analysis of root cause of failures is becoming exceedingly challenging. This course examines both traditional and recently developed tools and techniques for isolating defects on simple and advanced ICs and microelectronic devices.

Preparation and characterization for AC and DC parametric, cache, and logic failures at package and die level will be discussed. Electrical, thermal, magnetic, electron and ion beam, and photonic fault isolation techniques will be reviewed, such as logic diagnostics, TDR, SQUID, OBIRCH/TIVA, TRE, TLS, PEM, PICA, lock-in thermography and many others. The challenges of non-invasive probing and characterization of ‘non-visual defects’ are also covered. A number of case histories will be examined with capabilities and limitations of techniques demonstrated.

Learning Objectives. Upon completion of this course, the student should be able to:
• Cite the purpose and benefits of fault isolation and failure analysis.
• Determine key prerequisites like characterization and sample preparation.
• Examine the trade-offs between methods, fail modes, and sample form-factors.
• Describe the tools and techniques and the physical and electrical principles behind them.
• Decide which methods to use for package, parametric, cache, and logic failures.
• Identify the strengths and limitations of specific techniques.
• Assess the future viability of the methods into the deep nanoscale regime.

Who Should Attend?
This course is designed for test and debug personnel, failure analysts, and characterization, yield, and reliability analysis engineers, technicians, managers, and anyone who submits devices to, performs, or analyzes results from failure analysis laboratories. Researchers, developers, and vendors of fault isolation and related equipment and failure analysis tooling in general will also benefit.

About the Instructor:
David P. Vallett
PeakSource Analytical (www.peaksourcevt.com), Fairfax, VT, USA
Failure Analysis Engineer/Manager (retired) IBM Systems & Technology Group, Essex Junction VT, USA

Mr. Vallett has over 30 years engineering and management experience in CMOS characterization and failure analysis with the IBM Systems & Technology Group. He now performs SQUID and GMR magnetic current imaging at his company PeakSource Analytical, LLC. He holds the BS degree in electrical engineering from the University at Buffalo, NY, USA since 1982.
He is highly experienced in electrical and physical failure analysis of semiconductor devices and packaging assemblies with a specialization in fault isolation using optical, thermal, and magnetic imaging and stimulation techniques for characterization and isolation of defects. He was recognized with IBM's Outstanding Technical Achievement award for development of Picosecond Imaging Circuit Analysis (PICA) using time-resolved photon emission microscopy and is active in the application of SQUID and GMR magnetic microscopy.
Mr. Vallett is widely published in the Failure Analysis field with five best-paper awards and has lectured internationally on fault isolation, magnetic imaging, and analytical technology challenges in both micro and nanoelectronics. He holds twenty-seven US patents and is a senior member of the IEEE, a member of the Electronic Device Failure Analysis Society, and belongs to Tau Beta Pi - the National Engineering Honor Society. He is a past chair of the International SEMATECH Product Analysis Forum and was the 2008 General Chair for ISTFA - the International Symposium for Testing and Failure Analysis.